IN THE CLAIMS:

1-8 (Canceled).

9. (Currently Amended) A memory controller for controlling a memory having a plurality of banks, the memory controller comprising:

an arbitration circuit for arbitrating a memory access request from a plurality of blocks for ~~making access to~~accessing a~~the~~ memory ~~from a plurality of blocks,~~;

a command generation block for generating a memory command for a~~the~~ memory based on a control signal from the arbitration circuit~~,~~;

an address generation block ~~which receives~~for receiving a memory address from a~~the~~ block permitted to access by the arbitration circuit and ~~outputs~~for outputting a~~the~~ memory address to the memory~~,~~; and

a data latch block ~~which latches~~for latching either write data from the block permitted by the arbitration circuit ~~to access~~for accessing a memory ~~by the arbitration circuit~~ or read data from a~~the~~ memory and ~~passes~~passing data between a~~the~~ memory and the block ~~permitted to access~~, wherein

bank access data is access data to the memory~~, the access data having~~comprising a predetermined number of bytes for performing writing or reading on a~~the~~ same bank of the memory, block access data is a data unit ~~constituted of~~comprising two sets of the bank access data belonging to different banks, and ~~in the case where~~if the plurality of blocks make a memory access request for each piece of the block access data, when a second-half bank where memory

access is permitted immediately before is the same as the first-half bank of a subsequent memory access request, the arbitration circuit changes an order of memory access of the bank access data in the block access data~~.~~,

wherein the data latch block comprises:

a write data latch block for receiving and latching write data from the plurality of blocks;

a data change block for changing, based on a data latch control signal from the arbitration circuit, an order of bank access data outputted by the write data latch block, outputting the data as write data to the memory changes an order of bank access data outputted by a read data latch block, and outputting the data as read data to a block permitted to perform read access to the memory; and

a read data latch block which receives and latches the read data having been read from the memory.

10. (Currently Amended) The memory controller according to claim 9, wherein the arbitration circuit comprises:

a request receiving block ~~which receives~~for receiving a memory request and a memory address from the plurality of blocks, ~~includes~~the request receiving block comprising a bank decision unit for deciding, based on the received memory address, whether access is made to the same bank regarding a second-half bank where memory access has been permitted immediately before and a first-half bank of a subsequent memory access request, and ~~provides~~providing an instruction to generate an enabling signal~~,~~;

a memory access priority designating unit for designating priority of memory access from the plurality of blocks~~,~~;

an enabling signal generation block which is instructed by the request receiving block, ~~to generate~~for generating the enabling signal and ~~outputs~~outputting the enabling signal to the block permitted to access the memory~~,~~; and

a control signal generation block, which is instructed by the request receiving block, ~~to generate~~for generating the control signal ~~and generates each control signal~~.

11. (Canceled).

12. (Original) The memory controller according to claim 9, wherein when the second-half bank where memory access has been permitted immediately before is the same as the first-half bank of the subsequent memory access request, the arbitration circuit changes an order of the bank access data in the block access data, reads the block access data from the memory, and stores the data in the data latch block, and the data latch block changes an order of each piece of the bank access data in the block access data and transfers the data to the block having performed memory access.

13. (Currently Amended) The memory controller according to claim 10, wherein the memory access priority designating unit ~~can be~~is set from outside and the priority of access from the plurality of blocks to the memory ~~can be~~is changed according to a setting of the memory access priority designating unit.

14. (Original) The memory controller according to claim 9, wherein the memory is a synchronous memory.

15. (Currently Amended) A memory controller for controlling a memory having a plurality of banks, the memory controller comprising:

an arbitration circuit for arbitrating a memory access request from a plurality of blocks for ~~making access to~~ accessing a the memory ~~from a plurality of blocks,~~;

a command generation block for generating a memory command for ~~the~~a memory based on a control signal from the arbitration circuit~~,~~;

an address generation block ~~which receives~~for receiving a memory address from ~~the~~a block permitted by the arbitration circuit ~~to access~~for accessing a memory ~~by the arbitration circuit~~ and ~~outputs~~outputting the memory address to ~~the~~such memory~~,~~; and

a data latch block ~~which latches~~for latching either write data from the block permitted by the arbitration circuit ~~to access~~for accessing a memory ~~by the arbitration circuit~~ or read data from ~~the~~a memory and ~~passes~~passing data between ~~the~~a memory and the block ~~permitted to access~~, wherein

~~when~~ bank access data is access data to the memory~~, the access data having~~comprising a predetermined number of bytes for performing writing or reading on ~~the~~a same bank of the memory, block access data is a data unit ~~constituted of~~comprising two sets of the bank access data belonging to different banks, and the arbitration circuit instructs the command generation

block to provide a wait cycle when a memory access request is made by the bank access data alone from the block permitted to access the memory.

16. (Currently Amended) The memory controller according to claim 15, wherein the arbitration circuit comprises:

a request receiving block ~~which receives~~for receiving a memory request and a memory address from the plurality of blocks, ~~includes~~the request receiving block comprising a data unit decision unit for deciding a data unit of requested memory access based on the received memory request, and ~~provides~~providing an instruction to generate an enabling signal~~,~~;

a memory access priority designating unit for designating priority of memory access from the plurality of blocks~~,~~;

a wait cycle designating unit for designating the number of wait cycles provided when memory access is requested from the plurality of blocks by the bank access data alone,

an enabling signal generation block which is instructed by the request receiving block, ~~to generate~~for generating the enabling signal and ~~outputs~~outputting the enabling signal to the block permitted to access the memory~~,~~; and

a control signal generation block, which is instructed by the request receiving block, ~~to generate~~for generating the control signal ~~and generates each control signal~~.

17. (Currently Amended) The memory controller according to claim 16, wherein the memory access priority designating unit ~~can be~~is set from outside and the priority of access from

the plurality of blocks to the memory ~~can be~~is changed according to a setting of the memory access priority designating unit.

18. (Currently Amended) The memory controller according to claim 16, wherein the wait cycle designating unit ~~can be~~is set from outside and the number of wait cycles provided by the command generation block ~~can be~~is changed according to a setting of the wait cycle designating unit.

19. (Currently Amended) The memory controller according to claim 15, wherein the memory is a synchronous memory.

20-33 (Canceled).

34. (Currently Amended) A memory controller for controlling a memory having a plurality of banks, the memory controller comprising:

an arbitration circuit for arbitrating a memory access request from a plurality of blocks for ~~making access to~~ accessing a the memory ~~from a plurality of blocks,~~;

a command generation block for generating a memory command for ~~the~~a memory based on a control signal from the arbitration circuit~~,~~;

an address generation block ~~which receives~~for receiving a memory address from ~~the~~a block permitted by the arbitration circuit ~~to access~~for accessing a memory ~~by the arbitration circuit~~ and ~~outputs~~outputting the memory address to ~~the~~such memory~~,~~; and

a data latch block ~~which latches~~for latching either write data from the block permitted by the arbitration circuit ~~to access~~for accessing a memory ~~by the arbitration circuit~~ or read data from ~~the~~a memory and ~~passes~~passing data between ~~the~~a memory and the block ~~permitted to access~~,

wherein the arbitration circuit designates an arbitrating method for changing priority of memory access from the plurality of blocks when the memory access request from the plurality of blocks is made to the same bank as immediately preceding access and memory access permitted by the arbitration circuit immediately before is read access.

35. (Currently Amended) The memory controller according to claim 34, wherein the arbitration circuit comprises:

a bank decision unit ~~which receives~~for receiving a memory address from the plurality of blocks and ~~decides~~deciding whether access is made to the same bank ~~or not~~ based on the received memory address,

an access request decision unit ~~which receives~~for receiving a memory request from the plurality of blocks and ~~decides~~deciding the kind of requested memory access based on the received memory request,

a request receiving block which includes the bank decision unit and the access request decision unit and provides an instruction to generate an enabling signal,

a memory access priority designating unit for designating the priority of memory access from the plurality of blocks,

an arbitrating method designating unit for designating an arbitrating method for changing the priority of memory access when the memory access request from the plurality of blocks is

made to the same bank as immediately preceding access and memory access permitted by the arbitration circuit immediately before is read access,

an identical bank priority designating unit for selecting a block to be subsequently permitted to access when the arbitrating method designating unit is set so as to place higher priority on a bank,

a read access priority designating unit for selecting a block to be subsequently permitted to perform read access when the arbitrating method designating unit is set so as to place higher priority on access,

an enabling signal generation block which is instructed by the request receiving block ~~to generate~~for generating the enabling signal and ~~outputs~~outputting the enabling signal to the block permitted to access the memory, and

a control signal generation block which is instructed by the request receiving block ~~to generate~~for generating the control signal and ~~generate~~generating each control signal.

36. (Currently Amended) The memory controller according to claim 35, wherein the memory access priority designating unit ~~can be~~is set from outside and the priority of access from the plurality of blocks to the memory ~~can be~~is changed according to a setting of the memory access priority designating unit.

37. (Currently Amended) The memory controller according to claim 35, wherein the arbitrating method designating unit ~~can be~~is set from outside and the arbitrating method of

memory access from the plurality of blocks ~~can be~~is changed according to a setting of the arbitrating method designating unit.

38. (Currently Amended) The memory controller according to claim 35, wherein the identical bank priority designating unit ~~can be~~is set from outside and a block to be subsequently permitted to access to the memory ~~can be~~is selected according to priority set by the identical bank priority designating unit when the arbitrating method designating unit is set so as to place higher priority on a bank and a memory access request is made from the plurality of blocks to the same bank as immediately preceding access.

39. (Currently Amended) The memory controller according to claim 35, wherein the read access priority designating unit ~~can be~~is set from outside and a block to be subsequently permitted to perform read access to the memory ~~can be~~is selected according to priority set by the read access priority designating unit when the arbitrating method designating unit is set so as to place higher priority on access and memory access permitted by the arbitration circuit immediately before is read access.

40. (Original) The memory controller according to claim 34, the memory is a synchronous memory.